INSTITUTE OF PHYSICS PUBLISHING NANOTECHNOLOGY

Nanotechnology **17** (2006) 2203–2206 doi:10.1088/0957-4484/17/9/021

Contact characteristics in GaN nanowire devices

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Received 6 February 2006, in final form 1 March 2006
Published 31 March 2006
Online at stacks.iop.org/Nano/17/2203

Abstract

GaN nanowire field-effect transistors were fabricated using single-crystalline GaN nanowires synthesized by thermal evaporation of GaN powder with NH_3. They were found to be depletion mode transistors with an electron concentration of $\sim 10^7$ cm^{-1}, electron mobility of 50 cm^2 V^{-1} s^{-1}, and on/off current ratio of $\sim 10^2$. Using the transmission line method, the resistivity of the GaN nanowires and specific contact resistivity were estimated to be 7.8×10^{-2} Ω cm and 1.7×10^{-5} Ω cm^2, respectively. The current transport at contacts was described by the thermionic emission with a barrier height of 68 meV. The contact characteristics were improved by supplying excess carriers in the nanowires. These results will enable GaN nanowires to be used in reliable nanoscale devices.

1. Introduction

One-dimensional nanostructures such as nanowires, nanotubes, and nanobelts are of considerable interest due to their application potentials as building blocks for nanoelectronics and nanophotonics [1–3]. Among several III–V compound semiconductors, GaN has been extensively researched for use in short-wavelength photonic devices [4], high-power and high-temperature electronic devices [5], and room-temperature operating spintronic devices [6], owing to its superior properties such as high thermal conductivity and room-temperature ferromagnetism as well as direct wide bandgap of 3.4 eV at room temperature. Devices using GaN nanowires can improve device performances due to their unique physical properties such as high crystalline quality, large surface area, and quantum confinement effect. Recently, several groups have studied the synthesis of GaN nanowires using various methods such as arc discharge [7], laser ablation [8], sublimation [9], and chemical vapour deposition [10, 11], and their resulting characteristics. Although the performance of the nanowire devices is restricted by the contact resistance on the GaN nanowires, the electrical properties of the GaN nanowire contacts, such as specific contact resistivity and barrier height, have not been investigated in detail. In this study, GaN nanowires were configured as field effect transistors and then the carrier concentration and mobility were determined. The resistivity of the GaN nanowires and specific contact resistivity in GaN nanowire devices were investigated using the one-dimensional transmission line method (TLM). Moreover, the barrier height in GaN nanowire devices was studied by measuring the resistances as a function of temperature.

2. Experimental details

The GaN nanowires were synthesized by thermal evaporation of GaN powder (99.99%) in a horizontal tube furnace under high-purity NH_3 (99.999%) gas flow with a rate of 30 sccm at 600 mTorr. The temperature was raised to 1100 °C at a rate of 30 °C min^{-1} and was maintained for 30 min. Si(100) substrates coated with 0.1 M solution (solvent: ethanol) of nickel II acetate tetrahydrate ($Ni(Ac)_2 4H_2O$), which is a precursor of Ni nanoparticles, were located at the downstream of the furnace with a separation of about 100 mm from the sources, i.e. in the colder zone near the venting outlet. After the synthesis process, GaN nanowires with lengths up to 10 μm and diameters from 10 to 50 nm were obtained on the substrates. The crystal structure of the synthesized nanowires was analysed using high-resolution transmission electron microscopy (HRTEM).

In order to fabricate field-effect transistors (FETs), GaN nanowires were released from the substrates by sonication in isopropyl alcohol and subsequently transferred to a degenerately doped p-type Si substrate capped with a thermally grown 100 nm thick SiO_2 layer, where underlying Si was used

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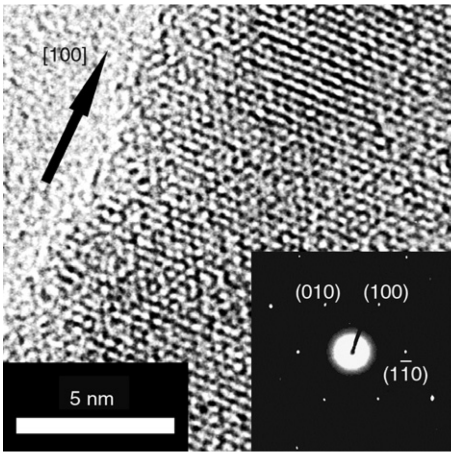

Figure 1. Representative HRTEM image and SAED pattern of a single GaN nanowire whose growth direction is along [100].

as a back gate. Then, the position of the randomly distributed nanowires on the substrate was confirmed using atomic force microscopy (AFM). After that, the source and drain electrodes were defined on the ends of the nanowires using electron beam lithography which was followed by sputtering of Ti/Au (20/50 nm). Since Ti/Au was deposited on the samples loaded on the rotating holder using 45°-tilt sputtering, it was assumed that the whole circumference of the nanowires was contacted. Finally, rapid thermal annealing was performed at 600 °C for 30 s in N_2 atmosphere. The channel length in the devices was controlled from 2 to 4 μm for TLM measurements of contact resistance. We have fabricated at least ten nanowire devices with identical channel length in which the maximum variation of the measured resistance is not orders of magnitude and the representative resistance was employed for TLM. These results demonstrate reproducibility in the fabrication of the nanowire devices.

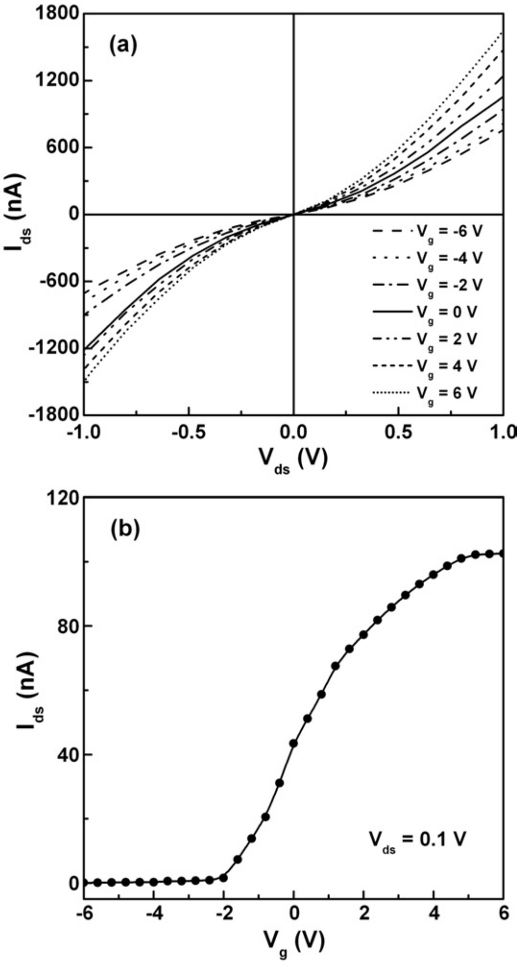

Figure 2. (a) I_{ds}–V_{ds} curves of GaN nanowire FET at different gate voltages. (b) Transfer characteristic of GaN nanowire FET at $V_{ds} = 0.1$ V.

3. Results and discussion

Figure 1 shows a representative HRTEM image of a single nanowire along with the corresponding selected area electron diffraction (SAED) pattern. In the HRTEM image of the GaN nanowire, (100) fringes with a spacing of 0.276 nm were found to be perpendicular to the edge of the nanowires. The HRTEM image and SAED pattern demonstrate that the nanowires have a single-crystalline GaN wurtzite structure with the growth direction along [100].

In the GaN nanowire FETs, the channel current versus drain-source voltage (I_{ds}–V_{ds}) characteristics at different gate voltages (V_g) and transfer characteristics (I_{ds}–V_g) were measured at room temperature, and the results are shown in figures 2(a) and (b), respectively. They showed that the conductance of the nanowires increased with increasing V_g and the on/off current ratio at the V_{ds} of 0.1 V exceeded 10^2 by changing the gate voltage from −6 to 6 V, indicating the typical characteristic of *n*-channel depletion mode FETs. The electron concentration, n, of the nanowire can be expressed as $n = CV_{th}/(e\pi r^2 L)$, where C is the nanowire capacitance, V_{th} is the gate threshold voltage, r is the nanowire radius, and L is the nanowire channel length [12]. The capacitance can be given by $C = 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$, where ε is the dielectric constant, ε_0 is the permittivity of free space, and h is the thickness of the SiO_2 dielectric layer [12]. Using $r = 25$ nm and $L = 2$ μm for the given nanowire FET, the electron carrier concentration was estimated to be $\sim 10^7$ cm^{-1}. In addition, the electron mobility, μ, can be estimated from the transconductance, $\mathrm{d}I/\mathrm{d}V_g = \mu(C/L^2)V_{ds}$, and it was calculated to be 50 cm^2 V^{-1} s^{-1} [12]. These are better than those of unintentionally doped GaN films grown directly on sapphires but are less than those of the films grown with an AlN buffer layer on sapphire [13]. This is attributable to point defects such as nitrogen vacancies and/or impurities and surface defects due to large surface area of nanowires, which act as the scattering centres in the channel.

To determine the resistivity of the GaN nanowires and the associated specific contact resistivity between the GaN nanowire and the Ti/Au electrodes, we employed the one-dimensional TLM formulae expressed as the following equation [14, 15]: $R_T = 2R_c + (\rho_s/\pi)(L/r^2)$, where R_T is the total resistance, R_c is the contact resistance, and ρ_s is the resistivity of the GaN nanowire. Figure 3 shows the total resistance obtained from the I–V characteristics for each nanowire device as a function of the channel length over the square radius of the nanowire (L/r^2). From the slope and the

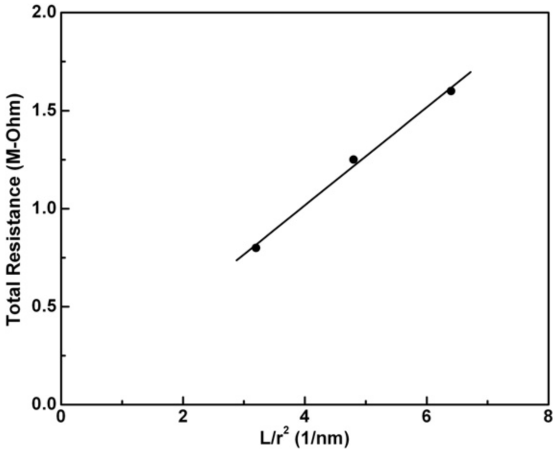

Figure 3. Total resistance of GaN nanowire devices as a function of the channel length over the square radius of the nanowire.

intercept of the linear fit, the resistivity of 7.8×10^{-2} Ω cm and the specific contact resistivity of 1.7×10^{-5} Ω cm^2 were determined, respectively. Such a specific contact resistivity is comparable to that of n-type GaN films annealed with similar conditions [16].

To examine the mechanisms which govern the current flow at the contacts between the GaN nanowire and the Ti/Au electrodes, the temperature dependence of resistance was measured and the results are shown in figure 4(a) on a semi-logarithmic scale. The resistance was found to increase monotonically with inverse temperature. This behaviour is in accordance with thermionic emission model [17] since the current representing thermionic emission can be proportional to $\exp(-\phi_B/k_BT)[\exp(qV_{ds}/k_BT) - 1]$, where ϕ_B is the barrier height, k_B is Boltzmann's constant, T is the absolute temperature, and q is the elementary charge. If the field emission were to dominate the current transport, the contacts between the GaN nanowire and the electrodes would become perfectly ohmic [17]. As is shown in figure 2(a), nonlinear I–V characteristics result from thermionic emission current, implying the existence of a Schottky barrier. From the slope of the linear fit in the semi-logarithmic plot, the barrier height was estimated to be 68 meV. Since the current can be expressed in a thermal activation form, $\exp(-E_a/k_BT)$, this represents the activation energy, E_a, which is related to a native defect or impurity ionization energy in GaN [18]. The value of 68 meV corresponds to shallow donor energy due to nitrogen vacancies [19], revealing that n-type conductivity of the nanowires is ascribed to nitrogen vacancies rather than surface states. This is in contrast to that of ZnO nanowires reported in a previous study [18].

In order to improve performance in nanowire FETs, the contact resistance should be reduced as much as possible so that perfect ohmic contact should be formed. The ohmic contacts can be improved by tuning the work function of the semiconductors or electrodes. For semiconductors, the work function is modulated through generation of excess carriers such as the extrinsic doping into the semiconductors or irradiation of light with a photon energy larger than their bandgap energy. Ultraviolet (UV) ($\lambda = 325$ nm) light was used to produce excess carriers in the GaN nanowires, and the I–V characteristics in the dark and under UV illumination are shown in figure 4(b). The difference between dark current and photocurrent is clearly observed. The photocurrent was twice as large as the dark current at a given applied bias. The figure also shows a linear characteristic with applied bias, indicating low resistance ohmic contact on the GaN nanowires. The UV light irradiation produces excess carriers in the GaN nanowire which narrows the depletion region at the interface between the nanowire and the metals enough to generate direct electron tunnelling, thereby increasing the current [16]. It is expected that similar behaviour is achieved by controlling the n-type conductivity by Si doping of which the ionization energy is about 27 meV and decreases with increasing doping level [20].

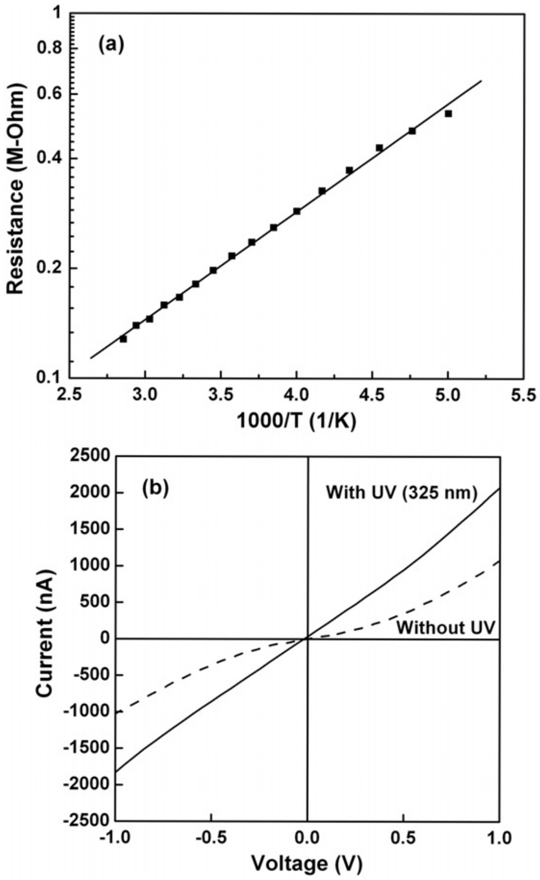

Figure 4. (a) Inverse temperature dependence of resistance of a GaN nanowire device. (b) I–V characteristics of a GaN nanowire device in the dark and under UV ($\lambda = 325$ nm) illumination.

4. Conclusion

In summary, the transport and contact characteristics in GaN nanowire FETs were investigated. The devices exhibit the characteristic of n-channel depletion mode transistors. In the devices, the resistivity of the nanowires and the specific contact resistivity were 7.8×10^{-2} Ω cm and 1.7×10^{-5} Ω cm^2, respectively, and thermionic emission current was dominant with a barrier height of 68 meV. The generation of excess carriers improved the ohmic contact on the GaN nanowires. The detailed studies of transport through nanowires and at contacts are expected to open up new opportunities towards potential applications of semiconductor nanowires in nanoelectronic, nanophotonic, and nanospintronic devices.

Acknowledgment

This work was supported by the National R&D Project for Nano Science and Technology.

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